Semiconductor and insulator nanostructures: challenges and opportunities

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Abstract

In the race to downsize integrated devices nanostructure fabrication is a primary challenge. Semiconductors and insulators technology has always relied on the top–down approach. Alternative "unconventional" approaches are now emerging, in particular the bottom-up approach. We describe recent work on the fabrication, patterning and integration of two important classes of new materials into the Si based technology, namely Ge/Si semiconductor hetero-structures and ABO_3 ferroelectric oxides.

Keywords: Nanostructured materials, Nanofabrication, Patterning, Unconventional approaches, Nanostenciling

1. Introduction

For over a decade different scientific communities have focused on the fabrication, processing and characterization of nanostructured materials. The semiconductor industry is looking to downsize the features of integrated devices in microelectronics [1], the optics community to build quantum dots (QDs) and wires, and the chemistry and biology communities to employ "self–assembly" methods capable of ordering molecular building blocks at the nanoscale [2].

The typical features of nanostructured materials fall in the size range ~1–100 nanometers (nm) and the fundamental study of phenomena that arise specifically from the critical size reduction of these systems belongs to the emerging field of Nanoscience. Such nanostructured materials are considered vital to the development of a number of promising technologies [3,4].

Research in semiconductor physics is presently driven by the aim of improving device performance. For most applications, nanostructure fabrication is the first major challenge. A second critical issue is the integration of new materials into conventional semiconductor technology – e.g. electroceramics into microelectronic integrated sensors, actuators or Micro Electro–Mechanical Systems (MEMS) [5], or Ge(Si) QDs on Si for QD mid-infrared photodectors, lasers or quantum cellular automata (QCA) [6].

In this article we describe recent work on the fabrication and integration of two important classes of materials into Si–based technology, namely Ge/Si semiconductor hetero–structures and ABO_3 ferroelectric oxides. We outline our approaches to fabricate and investigate patterned nanostructures of these two types of advanced materials.

2. Strategies to control nanostructure fabrication

2.1. 'Conventional' versus 'Non-conventional'

Top-down and bottom-up approaches are currently being explored to tailor structures at 1–100 nm scales. In top-down fabrication, a "bulk" material is progressively thinned down to obtain ever smaller features ("bulk" means that the starting material is continuous in all directions at a scale much larger than the structures of interest; typically this is a thin film). The "conventional" technique employed to manufacture integrated circuits is photolithography [7]. Modern photolithographic techniques can define structures of ~150–200 nm using ArF and F_2 excimer lasers (λ=193 nm and 157 nm respectively). Improving the resolution of this technique to tens of nanometers requires the use of smaller wavelengths for mask exposure (EUV (10–70 nm) or X–rays with wavelengths below 10 nm). So far, the trend towards device miniaturization sustained the development of advanced optical [8] and electron–beam lithography [9]. In turn, this increased enormously the fabrication cost of nanostructures.

Although such conventional routes are presently widely used, "unconventional" approaches are emerging as low–cost, high–resolution alternatives. Among unconventional approaches, let us mention soft lithography (micro–contact printing (μ–CP), replica molding (REM), micromolding in capillaries (MIMIC) [10] and nanoimprint lithography (NIL) [11-13]. These latter techniques are based on the mechanical transfer of a pattern from an elastomeric stamp or a hard mold to a substrate by direct contact.

The common drawback of these alternative solutions, as well as of all lithographic approaches, is that they require some type of resist or polymer process and consequently numerous chemical, thermal and etch associated steps.

Other unconventional approaches use controlled deposition to obtain nanoscale features. Among others, buffer–layer–assisted–growth (BLAG) [14] or laser–patterning (BLALP) [15], deposition on surfaces pre–patterned by laser interference [16] or focused ion beams (FIB) [17,18] represent other high–resolution and possibly low–cost patterning methods. Deposition through a miniature shadow–mask (nanostencil) [19] was lately also proposed as a flexible method to grow directly patterned nanostructures in a single step [20]. In section four we will elaborate on the versatility of this technique by presenting our work on the parallel fabrication and patterning of complex oxide nanostructures.

Besides the methods mentioned above, recent efforts have focused on a vastly different approach to create nanoscale structures, called bottom–up. This method exploits the natural tendency of atoms and molecules to assemble and form regular structures. However, controlling self–organization at this scale is challenging in itself.

2.2. 'Natural' versus 'Assisted' Self-organization

Self–organization represents the chief example of a bottom–up, parallel process. By exploiting the inherent characteristics of the substrate and deposited materials, as well as the laws of nucleation and growth, billions of nanoscale islands may be grown simultaneously. Their features can be tuned by varying kinetic parameters such as substrate temperature, total coverage, deposition rate and the post–growth thermal treatment. This represents a very attractive approach for applications, both because it is highly parallel and because it takes place without using artificial patterning, thus making it economically advantageous. This has prompted many experimental and theoretical efforts to understand and possibly control such processes [3,21].

However, several critical issues still prevent the full exploitation of self–organization. Since the functionality of a QD device relies on the electronic structure of the confined nanostructures, a narrow size and shape distribution is a crucial requirement. However, self–organization typically leads to broad (often multimodal) distributions, which yield a wide range of behaviors in a device. For example, the efficiency of a QD–based laser depends on the uniformity of electronic states separation within nanostructures across a dense array. The electronic structure of a QD depends on its size, shape, chemical composition and cristallinity, which in turn are all linked to its size [22,23]. The size evolution of

a 3D nucleus generally depends on its local environment, i.e. on its relative position with respect to the surrounding islands and their interactions.

The controlled positioning of nanostructures by a simple bottom–up approach is a challenging, if not unrealistic, task. In most cases the nucleation process occurs randomly and subsequent phenomena of ripening or coalescence do not cause a significant change in position [24]. Nonetheless, nanoscale ordering may be attained by harnessing the strain energy within a heteroepitaxial system. One remarkable example was demonstrated by burying an initially random array of 3D Ge islands on Si(001), and alternately overgrowing Si buffer layers and new layers of islands on top of it [25]. The tensile strain field prompts nucleation above buried islands, while progressively improving their order and their size uniformity (see Fig. 1).
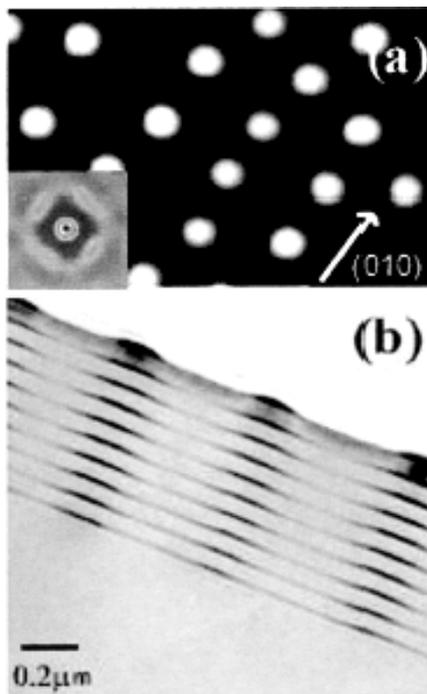

Fig. 1. Stacking Ge nano–islands on Si(001). (a): Atomic Force Microscopy image and (b): cross sectional TEM of a typical Ge/Si heterostructure. The structure was deposited at 750 °C. The inset of (a) shows the 2D autocorrelation function of a 100–μm² AFM image of the template surface showing the fourfold symmetry of the island arrangement (Courtesy of G. Capellini et al.[25]).

The features of the regularly spaced 3D structures can be tuned to some extent by varying growth parameters. Despite this outstanding achievement, the possibility of nano-pattern control is limited, preventing the application of this phenomenon to the design of complex architectures.

Overall, the self–organization of nanostructures is an exciting approach that merits further investigation to reach a better understanding of the processes taking place and to be able to control them.

Self–organization typically results in a random distribution or in an arrangement partly mirroring the incipient symmetry present in the buried layers. This is clearly insufficient for many applications, (non–volatile memories, QCA architectures).

Nevertheless, self–organization may be successfully exploited as the driving force for growing nanostructures on artificially patterned substrates. This approach, which we name assisted self–organization, will be described hereafter.

3. Ge/Si nanostructures, from bottom-up back to top-down

Low index crystallographic surfaces of Silicon are often used as substrates for the growth of Ge/Si nanostructures. Ge or Ge/Si nanocrystallites embedded within a Si matrix are expected to behave as traps for charge carriers, because of the narrower band gap of bulk Ge with respect to Si. As recipients of discrete quantities of electrical charge, these structures may be exploited as building blocks to design quantum bits in QCA architectures. Due to their low dimensionality and atomic–like electronic structure, they may also serve as light emitters or selective absorbers for new lasers or biosensors. The growth of Ge on Si surfaces has been the subject of extensive research during the past decade, the major factors justifying this interest being the relatively low cost of the prospective technology and the possibility of its integration with existing electronic devices.

The heteroepitaxial growth of lattice–mismatched materials often results in the self–organization of three–dimensional (3D) nanostructures on the substrate. Epitaxy requires the deposited material to reproduce the in–plane lattice features of the substrate material. This generally causes excess strain energy to be stored in the system, if the lattice parameters of the constituents are not matched. The

formation of 3D islands represents a possible pathway towards a partial strain release, since surface–roughening allows for some elastic relaxation. Two growth modes are frequently observed, commonly referred to as Stranski–Krastanov (SK) and Volmer–Weber (VW), respectively. In the first case (SK), after the completion of a flat and uniform wetting layer (WL), a roughening transition sets in through the nucleation and growth of 3D structures [26]. In the latter (VW), 3D islanding on the bare substrate occurs since the very beginning of the deposition process [27]. Island formation may be described in a simplified thermodynamic picture through the Young–Dupré equation [28], whereby the key factors governing the process are the surface and interface formation enthalpies. Although this description captures the essence of the phenomenon, reality is significantly more complicated, partially governed by atomic intermixing and point– and line–like defects that affect strain relaxation [22].
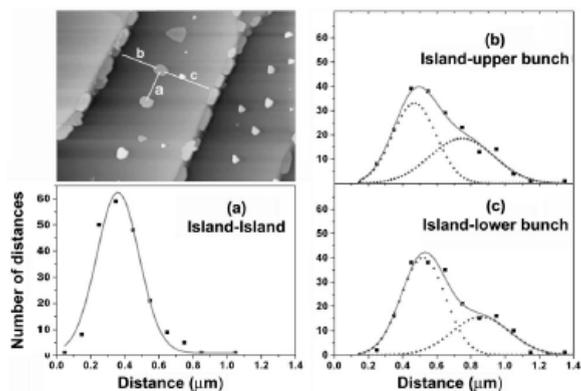

Fig. 2. Lateral ordering of Ge islands on the Si(111) step–bunched surface visible on the topographic STM image and quantified by statistical distributions. The analysis is performed on a sample covered by 8 monolayers of Ge deposited at 450 °C. (a): Island–island distance. (b): Island–upper bunch distance. (c): Island–lower bunch distance [31].

Germanium self–organizes on Si surfaces in nanoscale 3D islands, their shape depending on the crystallographic orientation of the substrate and the material volume within individual structures. In general, islanding occurs as a result of a SK process

[29], whereby surface roughening partially releases the strain energy due to the 4.2% lattice mismatch of Ge and Si. The most widely studied systems are Ge/Si(001) and Ge/Si(111). In both cases islands with different sizes and shapes are observed to coexist in a wide range of kinetic parameters and to be scattered randomly on the surface [30]. Numerous reports have proposed recipes to improve the spatial ordering and/or size uniformity of the islands, while an in–depth understanding of the origin and extent of the disarray is lacking. At present, the self–organization of Ge/Si islands does not provide satisfactory results for applications. Next, we will comment on a few selected examples showing how an increasing degree of top–down intervention yields an assisted self-organization that may lead to the design of Ge/Si–based devices. Model approaches combine self–organization and top–down, taking advantage of a predefined and adjustable array of defects at the substrate. An example of this is the growth of 3D Ge nanostructures on a step–bunched Si surface [31]. On these "pre–patterned" substrates, nucleation sites line–up along step bunches and in 1D row at terrace centers (see Fig. 2).

A similar phenomenon is observed by lithographically patterning Si substrates to artificially define an array of plateaus separated by steps or trenches on the surface, prior to Ge deposition. Several methods have been explored, some of which require pre–depositing a layer of Si oxide to be locally etched [32], whereas others rely on direct substrate patterning [33]. On these surfaces the growth of Ge follows a modified SK mode, since atomic diffusion is affected by the local arrangement of step–like defects. Depending on feature dimensions and growth kinetics, 3D islands preferentially nucleate on top of the plateaus, on the edges or within trenches. Alignment along the ridges is commonly observed, closely resembling the results obtained on step–bunched surfaces.

Though the process may well help understanding the local diffusion dynamics, it resorts to lithography with all its drawbacks, e.g. the lack of resolution for the desired complex architectures.

A noticeable improvement in this sense was obtained by 'digging' the Si surface by using a focused ion beam (FIB) [18] (See Fig. 3). While achieving an extraordinary lateral resolution (few

tens of nanometers) in the ditches localization, it does not induce a complete ordering of Ge islands. Not all the milled features act as nucleation sites for the islands, which are scattered all the way over the defined discrete network.
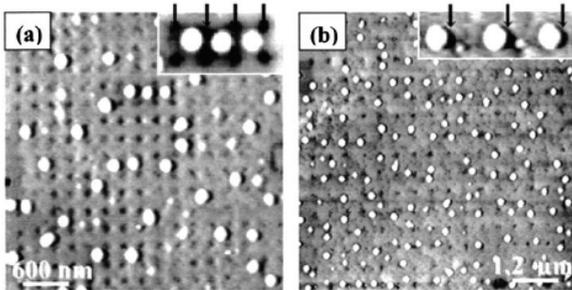

Fig. 3. Organization of Ge islands on a patterned Si(001) surface. Growth temperature: 700 °C; Ge thickness: 14 Å. The initial hole–diameter was 40 nm with a pitch of (a) 180 and (b) 350 nm. (Courtesy of A. Karmous et al. [18]).

All top–down methods presented so far are based on procedures that require surface patterning prior to deposition. Pre–patterned surfaces are then intended to influence diffusion processes so as to cause a predefined arrangement of preferential nucleation sites, thus dictating island size and ordering.

The approach that we are currently developing, still based on controlled deposition, relies however on a completely different and novel paradigm. We do not intervene on the Si substrate, but rather selectively deposit Ge directly on the sites where we would like the 3D islands to nucleate, even in a regime where otherwise a pure SK growth would take place. This in turn is expected to yield individual structures of optimum crystal quality and related electronic performance. Selective deposition is achieved by interposing a nanosieve between the bare Si surface and a Ge molecular beam. In the next section we elaborate on this approach and demonstrate how patterns milled in a nanomask can be successfully transferred to the substrate, and nanostructures of complex functional materials selectively deposited at desired locations. For this purpose we use a complex material, namely a ferroelectric oxide. The process is directly applicable to the deposition of arbitrary materials.

4. Ferroelectric oxides: the quest for functionality

Electroceramic materials can be defined as a family of ceramic materials that are used for their specific electrical, magnetic, or optical properties or a combination thereof (e.g. electro–mechanical, magneto–optical or electro–optical). Their properties can be tailored to serve as insulators, electrodes, piezoelectrics, pyrolectrics, ferroelectrics or high temperature superconductors (HTSC), thus providing a large number of options suitable for sensors and actuators, electronic components or MEMS [34,35].

Since the discovery of ferroelectricity in perovskites in the early 1940s, ferroelectric oxides have offered new solutions for technology and device applications [36]. These materials where first employed in $BaTiO_3$–based high dielectric capacitors, and later developed into piezoelectric transducers, positive temperature coefficient (PTC) devices and electro–optic light valves [37]. In brief, ferroelectrics are materials that exhibit, over a certain temperature range, a spontaneous electric polarization that can be reversed or reoriented by applying an electric field. This feature (i.e. the presence of a switchable electric polarization) can be used as bipolar logical states and ferroelectric oxides are thus ideal for applications in media for non–volatile storage [38], e.g. in non–volatile ferroelectric random access memories (NV–FeRAMs). Since all ferroelectric materials are also piezoelectric (an electrical polarization is produced within the crystals as a result of a mechanical strain and viceversa), the interest for ferroelectric ceramics expanded to employ them in the ever–growing field of MEMS. An extensive report concerning the integration of electroceramic materials into microelectronic components, microsensors and MEMS, as well as aspects induced by nanoscale size reduction (so–called size effects) has been previously presented [5].

For application purposes, ferroelectric thin films grown by various techniques such as sputtering, pulsed laser deposition, chemical solution deposition or thermal vapor deposition need to be micro– or even nanopatterned, a very challenging task because of their mechanical and chemical properties. The critical issue of patterning ferroelectric ceramic thin films for micro–sensors and micro–actuators is currently the subject of extensive research (see e.g. [39] for the standard micromachining processes used

to fabricate lead zirconate titanate piezoelectric thin film devices). There is thus a need to develop adequate patterning processes that avoid film degradation. Alternative techniques to traditional photolithography have been developed such as various soft lithography approaches (microtransfer printing, micromolding in capillaries, embossing and microcontact printing) mainly due to their low cost and high–throughput [40]. While most of these techniques have been demonstrated with resolution of ~100 nm, their inability to accurately register and align the patterns as part of a hierarchical fabrication scheme impeded their commercial implementation. These requirements are however necessary for the integration of ferroelectric oxides in microelectronics (e.g. see [41] for the requirements for a prospective 10 Gbit non–volatile ferroelectric memory). In addition, for a successful integration in microelectronics, more fundamental studies such as investigating size effects in ferroelectrics at the nanoscale are crucial [42] (the critical size is the smallest size at which the material is still ferroelectric. Since ferroelectricity is a "collective phenomenon", it collapses when the number of elemental dipoles is too small, as for ferromagnetism). The question arises whether an electroceramic cell with lateral sizes of 100 nm or below is still piezo– or ferroelectric.

Top–down nanoscale patterning methods such as focused ion beam (FIB), electron-beam direct writing (EBDW) or nano-imprint lithography (NIL) of ferroelectric oxides have recently been reviewed [43], also commenting on bottom up strategies (physical and chemical self–patterning of complex oxides) which promise even smaller features. It was concluded that bottom–up approaches are unreliable and not ripe for new technologies.

We will briefly describe here some results on NIL of ferroelectric materials. We argue that this technique is a reliable, promising alternative from the point of view of short term application in industry.

Standard NIL [11] employs a thermoplastic resist (polymer) which becomes viscous above its glass transition temperature and thus can be easily deformed by a hard mold (template). The first step consists in transferring the mold's pattern into the polymer film (sacrificial layer), creating a contrast thickness in the latter. After demolding, the residual

resist from the compressed areas is removed by reactive ion etching (RIE), and the patterned resist layer serves as an etching mask for subsequent feature transfer into the underlying material.

In some cases, the resist is itself a chemical precursor of the final material, which is directly obtained from the precursor after thermal treatment.

Harnagea et al. [44] prepared ferroelectric PZT cell arrays using a combination of chemical solution deposition and NIL. A precursor film was chemically spin–coated on a conductive substrate and patterned by pressing a nanostructured mold into it. The molds consisted of either macroporous silicon (prepared electrochemically) or of SiO_2–covered silicon wafers patterned by photolithography and RIE. After removing the mold, the precursor was crystallized into a ferroelectric oxide by drying and annealing.
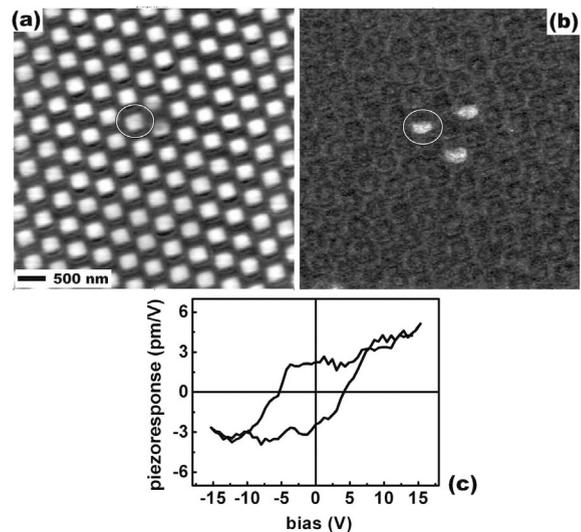

Fig. 4. Ferroelectric structures (250 nm in lateral size) and their behavior: (a) topography, z-scale 40 nm (b) PFM image showing three structures where polarization was switched upward (c) piezoresponse hysteresis loop of the cell circled in (a).

Arrays of ferroelectric cells with lateral sizes down to 250 nm were successfully prepared and their functionality was demonstrated by piezoresponse force microscopy (PFM) measurements (see Fig. 4). PFM tests the piezoelectric and switching properties of ferroelectric materials at the nanoscale, using a modified AFM [45,46].

We now describe in more detail our experimental results obtained with nanostenciling. This is a flexible top–down approach for surface patterning. Recently proposed as a flexible method to control the parallel patterning of nanostructures [19], it offers high versatility in the combination substrate/functional material and reduces the number of processing steps with respect to resist–based lithography. To date, deposition through nanostencils had been reported only for simple metals [20,47-50] and for NiO [51]. We deposited complex ferroelectric oxides [52] through silicon nitride stencil masks (nanostencils). Nanostencils with various sizes (nm and μm ranges) and shapes were fabricated by a combination of lithography or FIB and silicon micromachining.

The miniature shadow–masks were mechanically attached and temporarily fixed onto the substrate and the assembly substrate–stencil was mounted in a PLD deposition chamber, in front of a dense stoichiometric rotating target. Barium titanate, bismuth ferrite and lead zirconium titanate were chosen as materials to be selectively deposited through the mask. Rapid fabrication of ordered nanostructures was achieved in a single deposition step. Using stencils with circular holes (see Fig. 5a), ordered hexagonal arrays of dot–like $BaTiO_3$ structures were grown over the whole sieve areas (1 mm in length $\times$ 100 μm in width).

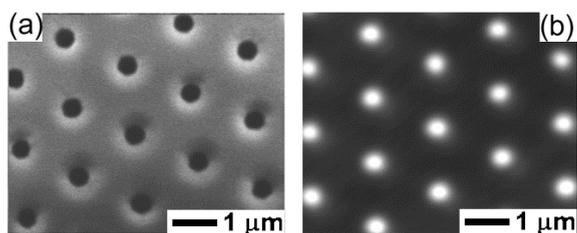*Fig. 5. (a) Scanning electron microscopy (SEM) image of a low-stress silicon nitride nanosieve with 300 nm diameter pores and 1.6 μm pitch (b) Tapping mode AFM image (height) of as-deposited $BaTiO_3$ nanostructures on Si(100) by PLD at room temperature through the periodic arrays of apertures made in the membrane [52].*

Figure 5 (b) shows the topography of the structures observed by tapping mode AFM. As–deposited $BaTiO_3$ nanostructures grown on Si(100)

have a dome shape with a height of 50 nm and a width of 400 nm (FWHM). A broadening of the bottom width of the structures, caused by the shadow–effect of the mask, occurs when the stencil is not pressed tightly enough against the substrate. Structures as small as 250 nm in width (FWHM) were obtained, the latter being reduced after several consecutive depositions through the same stencil.

A post–deposition annealing treatment (650 to 900 ºC for one hour in O_2 flow) was used to crystallize the structures. After annealing, the aspect of the dots changed from an amorphous dome-shape to an agglomeration of crystallites. XRD patterns obtained at grazing-angle incidence for the patterned structures and for the surrounding film area evidenced the presence of a polycrystalline phase very similar to the perovskite cubic phase.
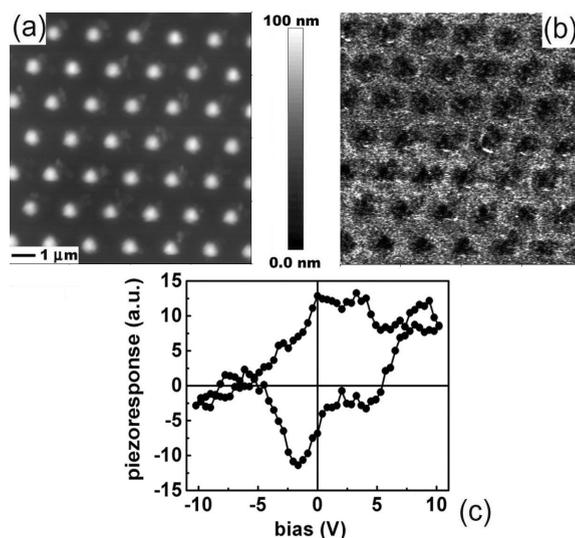

Figure 6: AFM and Piezoresponse Force Microscopy investigation of individual $BaTiO_3$ structures on a Nb–doped 100–oriented $SrTiO_3$ substrate (a) topography, (b) ferroelectric domain structure before switching and (c) switching piezoresponse hysteresis loop.

The ferroelectric nature of the $BaTiO_3$ nanostructures was probed by PFM. Figure 6 (a) presents the AFM topographical image of $BaTiO_3$ patterned on a Nb–doped $SrTiO_3(100)$ substrate together with the piezoresponse domain image recorded simultaneously (Fig. 6 (b)).

The dark regions reveal that the dots, as fabricated, have predominantly a spontaneous polarization oriented downward. The PFM signal was very weak, which is attributed to the reduced tetragonality of the $BaTiO_3$ unit cell caused by the fine grain size of the nanostructures (~30 nm). However, the piezoresponse hysteresis loop (Fig.6 (c)) reveals that the spontaneous polarization of the dots can still be switched and that the nanostructures retain ferroelectricity. This proves that not only the chemical composition and the crystal structure but also the functionality of the complex oxide nanostructures deposited through the nanostencils are conserved. Thus ferroelectricity in $BaTiO_3$ persists even at these small dimensions. This demonstrates the power of the nanostencil approach to both fabricate nanostructured complex functional materials and to investigate their growth and properties, and, furthermore, to enable the study of size effects on their functional properties.

Within the framework of these investigations, we plan to control the nanoscale positioning of other functional materials, including Ge QDs on Si.

5. Conclusions and Perspectives

Semiconductors and insulators technology has always relied on the top–down approach. The most remarkable example is the seemingly never ending miniaturization of transistors and microelectronic devices by ever more sophisticated lithographic techniques. Bottom–up self–organization has recently attracted much attention from the scientific community as a promising and appealing alternative. Self–organized nanostructures often exhibit excellent individual properties. However, the order and uniformity of collective ensembles of self–organized nanostructures is way too poor to be exploited for most applications such as integrated non–volatile memories or the structure of a logic circuit for QD–based QCA. Nevertheless, self–organization may be successfully exploited as the driving force for growing nanostructures specifically on an artificially designed template. The best–explored approach following this scheme consists in patterning a substrate prior to growth, so as to force the subsequent self–organization phenomena to reproduce the blueprint of the chosen artificial pattern

(assisted self–organization). We are currently exploring another path by depositing functional materials through a nanostencil, thus defining nucleation sites without affecting the substrate. We have shown how complex features drawn in a nanomask can be successfully transferred to the surface in the form nanostructures of complex functional materials, without otherwise intruding into the natural growth dynamics. On one hand it conserves the desired functionality of individual nanostructures; on the other it allows organizing them in the desired architectures. Our approach is highly flexible, serving for virtually any kind of materials and any kind of required feature arrangements. The further development of our strategy will pave the way to the realization of useful architectures and devices, contributing to move nanoscience towards nanotechnology.

Acknowledgements

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