Structural and electrical characterization of room temperature ultra-high-vacuum compatible SiO$_2$ for gating scanning tunneling microscope-patterned devices

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We present an ultrahigh vacuum technique for depositing SiO$_2$ at room temperature using an atomic oxygen source and Si coevaporation for ultimate use as a dielectric for gating Si devices with atomically precise dopant profiles. The resulting SiO$_2$ layers were characterized in situ by scanning tunneling microscopy, ex situ by transmission electron microscopy and ellipsometry and integrated as the gate dielectric in a metal oxide semiconductor field effect transistor (MOSFET). The electrical characteristics of the MOSFETs were investigated at 4.2 K, giving an interface trap density of $\sim 10^{11}$ cm$^{-2}$ eV$^{-1}$ from conductance and Hall effect measurements. © 2007 American Institute of Physics. [DOI: 10.1063/1.2815926]

Silicon devices with nano- to atomic scale dopant profiles have recently been realized using ultrahigh vacuum (UHV) scanning tunneling microscope (STM) lithography in combination with low temperature molecular beam epitaxy (MBE).$^{1,2}$ The strategy developed allows dopants to be placed in Si with atomic precision accuracy.$^{3}$ However, to gate and control the carrier density in these devices, a dielectric layer must be incorporated into the fabrication strategy with a very low thermal budget (down to room temperature) to avoid any dopant redistribution.$^{4}$ Ideally, the dielectric would also be fabricated under UHV to ensure a low level of impurities at the dielectric interface, and at low growth rates to ensure atomic precision control of the oxide thickness. In the semiconductor industry, a considerable effort has been devoted to reducing the temperature at which SiO$_2$ films are deposited to minimize dopant redistribution and preserve interfacial abruptness.$^{5}$ The most widespread low temperature oxidation technique is plasma-enhanced chemical vapor deposition (PECVD).$^{5}$ PECVD typically has a high growth rate of $\sim 50$ nm/min and as-grown films have high interface trap densities due to the significant incorporation of hydrogen from the source gases leading to the formation of Si–H and/or Si–OH at the SiO$_2$/Si interface. Postmetallization anneal treatments$^{6}$ have been used to reduce interface trap densities in SiO$_2$ layers prepared at $T=250$ °C by direct PECVD from as-grown values of $\sim 10^{13}$ cm$^{-2}$ eV$^{-1}$ down to $\sim 1.1 \times 10^{10}$ cm$^{-2}$ eV$^{-1}$.

In this letter, we investigate an alternative room temperature oxidation process that uses a neutral thermal atomic oxygen source and Si coevaporation under UHV conditions. Ultimately, this technique is compatible with devices which contain atomically precise dopant profiles patterned by STM.

Neutral atomic oxygen can oxidize silicon at temperatures down to room temperature due to its enhanced reactivity compared to molecular oxygen$^7$ without inducing surface damage typical of ion bombardment in PECVD. The deposition occurs in a controlled, low pressure UHV environment thereby minimizing the incorporation of unwanted background impurities in the film and allowing in situ analysis of the surface quality with the STM. We present a two-step growth strategy consisting of an initial exposure of the Si(100) surface to neutral thermal-energy atomic oxygen, followed by simultaneous Si codeposition under atomic oxygen exposure allowing atomic control over the growth. Such a two-step procedure separates and, therefore, allows independent optimization of the formation of the critical SiO$_2$/Si interface from the atomically controlled oxide deposition.

All oxidation experiments were performed on n-type Si(100) with a resistivity of 1–10 $\Omega$ cm. Samples were first chemically cleaned ex situ with a procedure described elsewhere$^8$ followed by introduction into UHV and an anneal at a $T \sim 500$ °C for several hours before rapidly flashing in situ to $\sim 1150$ °C while keeping the chamber pressure $\leq 5 \times 10^{-9}$ mbar. The as-flashed Si(100) surface was imaged by STM showing the characteristic $2 \times 1$ reconstruction with point defect densities below $\sim 2\%$. The samples were then transferred under UHV to a dedicated oxidation chamber (base pressure $2 \times 10^{-11}$ mbar), equipped with a resistive Si sublimation cell (SUSI), and a source of neutral thermal atomic oxygen extracted from a radio frequency (rf) plasma and operated at a rf power in the 200–500 W range. The two-step growth procedure starts with the $2 \times 1$ reconstructed Si(100) surface being exposed to a flux of atomic oxygen at pressure of $\sim 5 \times 10^{-6}$ mbar for 20 min. This causes a saturation of the surface state density giving an ultrathin SiO$_2$ layer ($\sim 0.6$ nm).$^9$ After 20 min, the second step commenced
with the SUSI shutter opened, resulting in the simultaneous delivery of atomic oxygen and Si to the sample surface. The growth process was then stopped by closing both Si and O source shutters simultaneously.

Figure 1(a) shows a STM image of a Si(100) surface after 5 min exposure to atomic O. We can see that the step structure characteristic of the Si(100) surface is maintained indicating the conformity of the oxidized surface to the underlying substrate, which suggests a layer by layer oxidation process. In addition, the granular texture observed is typical of ultrathin SiO$_2$, with bright regions related to tunneling through the oxide layer.

The samples were investigated ex situ by transmission electron microscopy (TEM) and variable angle spectroscopic ellipsometry (SE). Figures 1(c) and 1(d) show typical TEM micrographs of a 25-nm-thick SiO$_2$ layer grown at room temperature (rf power 200 W and growth rate of $\sim$0.20 nm/min). The higher-resolution TEM micrograph shows a sharp interface between the substrate and the oxidized material. The interface is defined as the region of abrupt change in electron density contrast across the SiO$_2$ layer.

The growth rate was determined from the thickness measured with TEM and etch step profiling, which give compatible results. Under typical oxidation conditions, growth rate of 0.15 nm/min is achieved, much lower than that found in the literature for PECVD techniques (typically 5–50 nm/min). Such slow growth rates are critical for forming uniform, dense SiO$_2$ layers when low substrate temperature deposition is used. To gain insight into the overall quality of the oxide layers, the same samples were investigated ex situ by variable angle SE. The SE data were analyzed by modeling the samples as an overlayer of stoichiometric SiO$_2$ (refractive index $n=1.462$) with thickness $t$ on top of the bulk Si substrate. The SE spectra mainly reflect the density of states of bulk Si, which is close to the band gap of bulk Si. This is consistent with results from TEM and etch step profiling analysis. Independently, the stoichiometry of the SiO$_2$ films was confirmed by modeling the overlay as a dispersion of a nonfully-oxidized material of volume fraction $f$ in bulk SiO$_2$. By analyzing the variable angle ellipsometry data using both $t$ and $f$ as independent fit parameters and repeating the fitting procedure for different kinds of nonfully-oxidized material (Si monoxide and amorphous Si), we found that $t$ is compatible with TEM measurements and $f \sim 0.1\% – 0.5\%$. This low value of $f$ (comparable with the detection limit of the technique) indicates that there is a low impurity content in the silicon dioxide layer grown and allows us to estimate a refractive index of $n=1.458 \pm 0.016$, comparable with the value $n=1.462$ quoted for stoichiometric SiO$_2$.

To validate the electrical properties of the oxide layers, we integrated them as gate dielectrics in a metal oxide semiconductor field effect transistor (MOSFET) using a Hall bar geometry. To achieve this, we have developed a complete UHV-compatible MOSFET process, as shown in Fig. 2. First, the source-drain regions and voltage probe contacts of the $n^+-n-n^+$ Hall bar MOSFET are defined by phosphorus diffusion in the substrate [Fig. 2(a)]. After the contacts were formed, the thermal oxide mask was etched away and the samples cleaned with a procedure described elsewhere. These $n^+-n-n^+$ MOSFET templates [Fig. 2(b)] were then loaded into UHV and rapidly flashed to $\sim 1150 \, ^\circ C$ to remove the thin native oxide and prepare the Si(100) 2 $\times$ 1 surface [Fig. 2(c)]. After the flashing and the investigation of the surface with STM, the oxide layers were grown using the same two-step oxidation procedure described above [Fig. 2(d)]. After removing the oxidized samples from UHV, the Ohmic contacts were defined by an aluminum metallization step [Fig. 2(e)] and annealed for 20 min at $T=350 \, ^\circ C$ in forming gas (95% N and 5% H). Finally, the gate electrode was also defined by an aluminum metallization [Fig. 2(e)]. Postmetallization annealing, which is a standard procedure to reduce interface trap densities, was avoided at this stage in order to gain insight on the quality of the as-grown oxides.

Electrical characterization of the $n^+-n-n^+$ Hall bar MOSFETs (channel width to length ratio of 10 $\mu$m/80 $\mu$m) was performed at 4.2 K using both dc and low frequency ac lock-in techniques. Due to the requirement of using conducting substrates for STM imaging, low temperature characterization of the MOSFET is necessary to freeze out substrate conduction (which occurs at $T>50 \, ^\circ K$). In Fig. 3(a), we present the transfer characteristics showing the modulation of the drain current $I_D$ as a function of the gate voltage $V_G$ measured at a fixed source-drain bias for a 40-nm-thick oxide grown at room temperature. We estimate a threshold voltage for conductance $V_T \sim 1.9 \, ^\circ V$. The leakage current $I_L$ from...
the interface is independently controlled from the bulk SiO2 density of a MOSFET characteristic, where the formation of that trap density achieved, calculated from the critical density $n_T = 4.4 \times 10^{11} \text{ cm}^{-2}$ is determined.

In summary, we have demonstrated the viability of a room temperature UHV-compatible SiO2 growth technique using atomic oxygen and Si coevaporation. With low growth rates of 0.2 nm/min, homogeneous SiO2 layers are formed with a sharp interface with the underlying Si substrate. As a proof of principle, we fabricated MOSFET devices integrating room temperature deposited SiO2 layers as a gate dielectric and tested them at 4.2 K, finding an electrically active trap density in the mid-$10^{11}$-cm$^{-2}$. An advantage of this technique is that it is UHV compatible, low-thermal budget, capable of integration with the STM/MBE based fabrication scheme for atomically precise devices in Si and, therefore, has the potential to expand this planar technology to a three-dimensional multilayer-architecture scheme.

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