Structural and electrical characterization of room temperature ultra-high-vacuum compatible SiO_2 for gating scanning tunneling microscope-patterned devices

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We present an ultrahigh vacuum technique for depositing SiO_2 at room temperature using an atomic oxygen source and Si coevaporation for ultimate use as a dielectric for gating Si devices with atomically precise dopant profiles. The resulting SiO_2 layers were characterized *in situ* by scanning tunneling microscopy, *ex situ* by transmission electron microscopy and ellipsometry and integrated as the gate dielectric in a metal oxide semiconductor field effect transistor (MOSFET). The electrical characteristics of the MOSFETs were investigated at 4.2 K, giving an interface trap density of $\sim 10^{11}$ cm^{-2} from conductance and Hall effect measurements. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2815926]

Silicon devices with nano- to atomic scale dopant profiles have recently been realized using ultrahigh vacuum (UHV) scanning tunneling microscope (STM) lithography in combination with low temperature molecular beam epitaxy (MBE).[1,2] The strategy developed allows dopants to be placed in Si with atomic precision accuracy.[3] However, to gate and control the carrier density in these devices, a dielectric layer must be incorporated into the fabrication strategy with a very low thermal budget (down to room temperature) to avoid any dopant redistribution.[4] Ideally, the dielectric would also be fabricated under UHV to ensure a low level of impurities at the dielectric interface, and at low growth rates to ensure atomic precision control of the oxide thickness. In the semiconductor industry, a considerable effort has been devoted to reducing the temperature at which SiO_2 films are deposited to minimize dopant redistribution and preserve interfacial abruptness.[5] The most widespread low temperature oxidation technique is plasma-enhanced chemical vapor deposition (PECVD).[5] PECVD typically has a high growth rate of ~50 nm/min and as-grown films have high interface trap densities due to the significant incorporation of hydrogen from the source gases leading to the formation of Si–H and/or Si–OH at the SiO_2/Si interface. Postmetallization anneal treatments[6] have been used to reduce interface trap densities in SiO_2 layers prepared at $T=250$ °C by direct PECVD from as-grown values of $\sim 10^{12}$ cm^{-2} eV^{-1} down to $\sim 1.1 \times 10^{10}$ cm^{-2} eV^{-1}.

In this letter, we investigate an alternative *room temperature* oxidation process that uses a neutral thermal atomic oxygen source and Si coevaporation under UHV conditions. Ultimately, this technique is compatible with devices which contain atomically precise dopant profiles patterned by STM. Neutral atomic oxygen can oxidize silicon at temperatures down to room temperature due to its enhanced reactivity compared to molecular oxygen[7] without inducing surface damage typical of ion bombardment in PECVD. The deposition occurs in a controlled, low pressure UHV environment thereby minimizing the incorporation of unwanted background impurities in the film and allowing *in situ* analysis of the surface quality with the STM. We present a two-step growth strategy consisting of an initial exposure of the Si(100) surface to neutral thermal-energy atomic oxygen, followed by simultaneous Si codeposition under atomic oxygen exposure allowing atomic control over the growth. Such a two-step procedure separates and, therefore, allows independent optimization of the formation of the critical SiO_2/Si interface from the atomically controlled oxide deposition.

All oxidation experiments were performed on *n*-type Si(100) with a resistivity of 1–10 Ω cm. Samples were first chemically cleaned *ex situ* with a procedure described elsewhere[8] followed by introduction into UHV and an anneal at a $T \sim 500$ °C for several hours before rapidly flashing *in situ* to ~1150 °C while keeping the chamber pressure $\leqslant 5 \times 10^{-9}$ mbar. The as-flashed Si(100) surface was imaged by STM showing the characteristic 2×1 reconstruction with point defect densities below ~2%. The samples were then transferred under UHV to a dedicated oxidation chamber (base pressure 2×10^{-11} mbar), equipped with a resistive Si sublimation cell (SUSI), and a source of neutral thermal atomic oxygen extracted from a radio frequency (rf) plasma and operated at a rf power in the 200–500 W range. The two-step growth procedure starts with the 2×1 reconstructed Si(100) surface being exposed to a flux of atomic oxygen at pressure of $\sim 5 \times 10^{-6}$ mbar for 20 min. This causes a saturation of the surface state density giving an ultrathin SiO_2 layer (~0.6 nm).[9] After 20 min, the second step commenced

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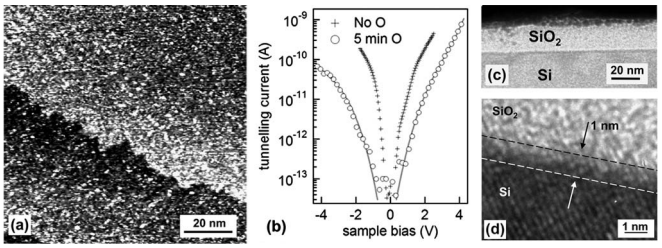

FIG. 1. (a) STM image (V_{sample}=3.5 V) of a Si(100) surface after 5 min exposure to atomic O. (b) STS *I-V* characteristics of clean Si(100) (crosses) and the same surface exposed to atomic O for 5 min (circles). The continuous lines are guides to the eye. [(c) and (d)] Cross-sectional bright field TEM micrographs of a 25-nm-thick oxide layer deposited at a growth rate of ~0.2 nm/min.

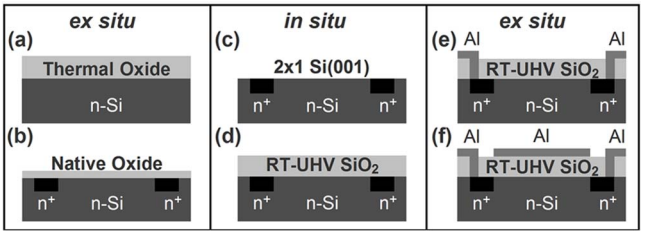

FIG. 2. *Ex situ* and *in situ* fabrication steps of a UHV-compatible MOSFET process. [(a) and (b)] First, a *n*-doped Si(100) wafer is patterned with n^+ phosphorus in-diffused regions to act as S-D regions using a thick thermal oxide mask. [(c) and (d)] The sample is then loaded into UHV to prepare the clean, reconstructed Si(100) 2×1 surface before the RT-UHV SiO_2 layer is grown in a two-step process. [(e) and (f)] The sample is removed from UHV and processed *ex situ* for Ohmic and gate contacts.

with the SUSI shutter opened, resulting in the simultaneous delivery of atomic oxygen and Si to the sample surface. The growth process was then stopped by closing both Si and O source shutters simultaneously.

Figure 1(a) shows a STM image of a Si(100) surface after 5 min exposure to atomic oxygen. We can see that the step structure characteristic of the Si(100) surface is maintained indicating the conformity of the oxidized surface to the underlying substrate, which suggests a layer by layer oxidation process.[10] In addition, the granular texture observed is typical of ultrathin SiO_2, with bright regions related to tunneling through the oxide layer.[10] Figure 1(b) shows a scanning tunneling spectroscopy (STS) measurement of the Si(100) surface prior to, and after, exposure to 5 min of atomic oxygen. In the *I-V* characteristics, the tunneling gap is observed to widen, after oxygen exposure, to ~1.5 eV which is close to the band gap of bulk Si. This is consistent with the Si(100) surface being fully oxidized and the STS spectra mainly reflecting the density of states of bulk Si.[9]

The samples were investigated *ex situ* by transmission electron microscopy (TEM) and variable angle spectroscopic ellipsometry (SE). Figures 1(c) and 1(d) show typical TEM micrographs of a 25-nm-thick SiO_2 layer grown at room temperature (rf power 200 W and growth rate of ~0.20 nm/min). The higher-resolution TEM micrograph shows a sharp interface between the substrate and the oxide layer with a good overall layer homogeneity and interface roughness of less than 1 nm. This sharpness of the interface compares well with other thermal oxides[11] and is better than low temperature PECVD oxides where the interfaces typically have ~2 nm roughness.[12] The growth rate was determined from the thickness measured with TEM and etch step profiling, which give compatible results. Under typical oxidation conditions, growth rate of 0.15 nm/min is achieved, much lower than that found in the literature for PECVD techniques (typically 5–50 nm/min). Such slow growth rates are critical for obtaining uniform, dense SiO_2 layers when low substrate temperature deposition is used.[5] To gain insight into the overall quality of the oxide layers, the same samples were investigated *ex situ* by variable angle SE. The SE data were analyzed by modeling the samples as an overlayer of stoichiometric SiO_2 (refractive index n=1.462) with thickness t on top of the bulk Si substrate at a wavelength of 632.8 nm, angle of 75° and leaving t as a variable fitting parameter. Satisfactory fitting was found for t values in agreement with results from TEM and etch step profiling analysis. Independently, the stoichiometry of the SiO_2 films was confirmed by modeling the overlayer as a dispersion of a nonfully-oxidized material of volume fraction f in bulk SiO_2. By analyzing the variable angle ellipsometry data using both t and f as independent fit parameters and repeating the fitting procedure for different kinds of nonfully-oxidized material (Si monoxide and amorphous Si), we found that t is compatible with TEM measurements and $f\sim0.1\%-0.5\%$. This low value of f (comparable with the detection limit of the technique) indicates that there is a low impurity content in the silicon dioxide layer grown and allows us to estimate a refractive index of $n=1.458\pm0.016$, comparable with the value n=1.462 quoted for stoichiometric SiO_2.

To validate the electrical properties of the oxide layers, we integrated them as gate dielectrics in a metal oxide semiconductor field effect transistor (MOSFET) using a Hall bar geometry. To achieve this, we have developed a complete UHV-compatible MOSFET process, as shown in Fig. 2. First, the source-drain regions and voltage probe contacts of the n^+-n-n^+ Hall bar MOSFET are defined by phosphorus diffusion in the substrate [Fig. 2(a)]. After the contacts were formed, the thermal oxide mask was etched away and the samples cleaned with a procedure described elsewhere.[8] These n^+-n-n^+ MOSFET templates [Fig. 2(b)] were then loaded into UHV and rapidly flashed to ~1150 °C to remove the thin native oxide and prepare the Si(100) 2×1 surface [Fig. 2(c)]. After the flashing and the investigation of the surface with STM, the oxide layers were grown using the same two-step oxidation procedure described above [Fig. 2(d)]. After removing the oxidized samples from UHV, the Ohmic contacts were defined by an aluminum metallization step [Fig. 2(e)] and annealed for 20 min at T=350 °C in forming gas (95% N and 5% H). Finally, the gate electrode was also defined by an aluminium metallization [Fig. 2(e)]. Postmetallization annealing, which is a standard procedure to reduce interface trap densities, was avoided at this stage in order to gain insight on the quality of the as-grown oxides.

Electrical characterization of the n^+-n-n^+ Hall bar MOSFETs (channel width to length ratio of 10 μm/80 μm) was performed at 4.2 K using both dc and low frequency ac lock-in techniques. Due to the requirement of using conducting substrates for STM imaging, low temperature characterization of the MOSFET is necessary to freeze out substrate conduction (which occurs at $T>50$ K). In Fig. 3(a), we present the transfer characteristic showing the modulation of the drain current I_{DS} as a function of the gate voltage V_G measured at a fixed source-drain bias for a 40-nm-thick oxide grown at room temperature. We estimate a threshold voltage for conductance $V_T\sim1.9$ V. The leakage current I_G from

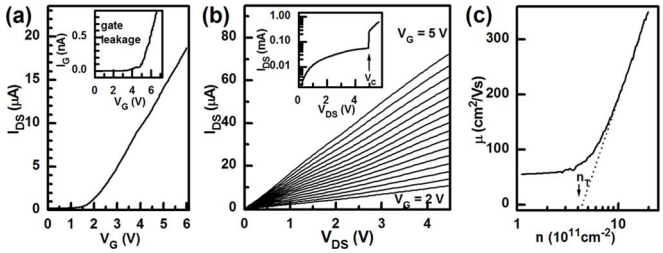

FIG. 3. Electrical characterization at $T=4.2$ K of a Hall bar geometry MOSFET incorporating a 40-nm-thick SiO_2 layer grown at room temperature at a rate of ~0.25 nm/min. (a) I_{DS}-V_G transfer characteristic measured at a $V_{DS}=900$ mV and, inset, gate leakage. (b) I_{DS}-V_{DS} output characteristics as a function of gate bias above threshold for the conduction for $V_G=2-5$ V. Inset: a curve measured at $V_G=4$ V over an extended V_{DS} range is reported showing the "kink" effect. (c) Mobility-density curve from which an electric active trap density $n_T=4.4\times10^{11}$ cm^{-2} is determined.

the gate through the oxide as a function of the gate bias V_G is shown as an inset in Fig. 3(a). A good insulating behavior of the gate oxide is evidenced by leakage currents of less than 100 pA for gate voltages $V_G<5$ V, which for this sample corresponds to an electric field through the dielectric of 1.25 MV/cm.

In Fig. 3(b), we report the transistor output characteristics, a series of I_{DS}-V_{DS} curves measured sweeping the source-drain voltage in the 0–4.5 V range at a rate of 0.05 V/s and progressively increasing the gate voltage from 2 to 5 V in steps of 0.2 V. Over the range of V_{DS} investigated the curves show near linear behavior, with the slope of the curves increasing as the gate voltage is increased. The slight deviations from linearity observed at low source-drain might be due to charge emission from shallow traps caused by the presence of a thin transitional layer present at the Si/SiO_2 interfaces, as suggested previously in low temperature studies of MOSFETs.[13] We restrict the source-drain bias range of up to 4.5 V since at higher biases, we observe the well known "kink effect" where the drain current shows an abrupt increase above a critical voltage V_C.[14] An example of such behavior is shown in the inset of Fig. 3(b) where the source-drain current measured at fixed $V_G=4$ V is shown up to 6 V. The arrow in the inset highlights the abrupt transition which occurs at $V_C=5$ V, beyond the expected pinch-off voltage $(V_G-V_T)\sim2.1$ V.

We estimate the density of electrically active traps present at the SiO_2/Si interface at 4.2 K from the mobility μ versus carrier density n curve obtained from the relation $\mu=1/(\rho ne)$ by measuring independently—as a function of gate voltage V_G—both the four-terminal resistivity $\rho(V_G)$ and, with the Hall effect, the carrier density $n(V_G)$.[15] In Fig. 3(c), we report on a logarithmic scale a typical μ versus n curve for a 40-nm-thick oxide MOFSET. The critical density n_c below which no conduction occurs due to freeze-out of free carriers due to impurity binding was determined by extrapolating to zero the linear drop of μ. We found $n_C=4.4\times10^{11}$ cm^{-2} and we assume it to be equal to the density n_T of the electrically active trap at the Si/SiO_2 interface.[15] We note that the trap density achieved, calculated from the critical density of a MOSFET characteristic, where the formation of the interface is independently controlled from the bulk SiO_2 deposition, is similar to that reported in the literature for SiO_2 layers grown at room temperature with a superlattice approach and measured using capacitance-voltage techniques.[16] Future attempts to reduce the trap density of the films will include higher substrate temperatures and *in situ* postoxidation and/or *ex situ* anneal steps after gate metallization.

In summary, we have demonstrated the viability of a room temperature UHV-compatible SiO_2 growth technique using atomic oxygen and Si coevaporation. With low growth rates of 0.2 nm/min, homogeneous SiO_2 layers are formed with a sharp interface with the underlying Si substrate. As a proof of principle, we fabricated MOSFET devices integrating room temperature deposited SiO_2 layers as a gate dielectric and tested them at 4.2 K, finding an electrically active trap density in the mid-10^{11}-cm^{-2}. An advantage of this technique is that it is UHV compatible, low-thermal budget, capable of integration with the STM/MBE based fabrication scheme for atomically precise devices in Si and, therefore, has the potential to expand this planar technology to a three-dimensional multilayer-architecture scheme.

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