Ambipolar operation of hybrid SiC-carbon nanotube based thin film transistors for logic circuits applications

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We report on the ambipolar operation of back-gated thin film field-effect transistors based on hybrid n-type-SiC/p-type-single-walled carbon nanotube networks made with a simple drop casting process. High-performances such as an on/off ratio of 105, on-conductance of 20 μS, and a subthreshold swing of less than 165 mV/decades were obtained. The devices are air-stable and maintained their ambipolar operation characteristics in ambient atmosphere for more than two months. Finally, these hybrid transistors were utilized to demonstrate advanced logic NOR-gates. This could be a fundamental step toward realizing stable operating nano-electronic devices. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4739939]

In recent years, thin-film transistors (TFTs) technology has undergone significant developments for applications in logic systems, especially for advanced electronic applications such as radio frequency identification tags and flat panel displays.1–5 Due to the excellent properties of silicon carbide (SiC), such as wide band-gap, high electron saturation drift velocity, and high thermal conductivity, transistor devices based on SiC have been studied extensively.6 Moreover, SiC is a wide-band-gap semiconductor on which a high quality thermal oxide of SiO2 can be grown. For example, 4H–SiC, with its high band gap of ~3.2 eV, could function well in a wide band-gap heterostructure as logic circuit if combined with a suitable complementary material. Among the various molecular switching units suggested to date as a)Authors to whom correspondence should be addressed. Electronic addresses: brahim.aissa@mpbc.ca and rosei@emt.inrs.ca.
Wire™) indicating a clear scattering radial breathing mode (RBM) peaks centered at 185 cm⁻¹ and attributed to the strong presence of SWNTs having a mean diameter of 1.2 nm, in total agreement with TEM observations. All the devices were fabricated on the epitaxial layer (P⁺ ion implantation was used with concentrations of 5 × 10²⁰ cm⁻³) deposited on the (0001) Si-face of 4H-SiC wafers, purchased from Cree, Inc. Detailed processing steps can be found elsewhere. To induce the electrical activation of the impurities and to crystallize the film, the implanted samples were annealed in a high vacuum furnace (2 × 10⁻⁶ mbar) at 1200 °C during 2 h. Samples were then oxidized for 13 h in dry O₂ at 1150 °C, yielding a gate dielectric oxide of about 110 nm. They were subsequently annealed in NO at 1175°C for 4 h. Prior to SWNT deposition, the SiO₂ was first chemically etched from one side (hydrofluoric acid 13% with an etching rate of 4.43 nm/min). Figure 1(c) shows the contact-mode atomic force microscopy images (NanoScope III, Digital Instrument) of the SiC surface after SiO₂ removing. The purified SWNTs were first ultrasonicated in dimethylformamide (1 mg/ml) solution for 5 h to dissolve the SWNT bundles. The solution was then centrifuged at 12300 rpm for 15 min to select well-dispersed, narrow bundles of the SWNTs. The centrifuged solution was then drop (10 μl) casted on the top of n-4H-SiC surface (held at 50 °C for solvent evaporation). The density of deposited SWNTs was controlled through the number of drops cast on the substrate. Ti/Au (20/180 nm) drain, source, and back-gated electrodes were then deposited by means of PLD (pulsed laser deposition, using ArF excimer laser, 193 nm) in a TFT scheme (Fig. 1(d)). Finally, a thin film of PMMA (Miller-Stephenson Chemical Co., Inc.) was directly deposited (by drop coating) onto the nanotubes network, to spatially maintain the SWNTs’ percolation distribution and to protect the TFT active channel from long term oxidation. Electrical transport properties of our hybrid TFTs were measured using a semiconductor parameter analyzer HP4155C, Agilent Technologies.

The channel length and width were initially designed to be 5 and 50 μm, respectively. To remove the metallic-SWNTs, we introduced an electrical breakdown (more details on the process are available in Ref. 25). Hereafter, we discuss the device characteristics achieved after the breakdown procedure. The on/off transistor switching ratios undergo significant improvement but are inevitably accompanied by a significant degradation of the on-current. Nevertheless, the electrical breakdown is time consuming, and thus one still needs to develop better ways to scale up the removal of metallic nanotubes.

We carried out systematic studies of the electrical performance of the devices. Figure 2(a) shows the TFT transfer
characteristics (conductance $G$ as a function of gate voltage $V_G$) at 100 mV drain voltages ($V_{DS}$) measured in air (for a TFT channel length of 5 $\mu$m). All devices exhibit clear ambipolar characteristics, showing that one branch (p-type) of $I_{DS}$ (or $G$) results from hole injection from the source, while the other branch (n-type) is due to electron injection from the drain. For the sake of discussion, we denote that the TFTs exhibit low off-conductance ($G_{OFF} < 1$ nS) measured at off-state and high on-conductance ($G_{ON} > 20$ $\mu$S) measured at the on-states for both the p- and n-regions. The corresponding on/off switching ratio was found to be as high as $10^5$, with an excellent subthreshold swing $S$ of 165 and 125 mV/dec, for the n and p TFT-regions, respectively. Our hybrid TFTs exhibit very promising characteristics rarely observed simultaneously.

At the On-states TFTs, we measured the average on-resistances of the devices (expressed as the average of the on-resistances of both the p- and n-regions, respectively) as a function of the transistor channel lengths. Such devices were made with channel widths $W$ of 50 $\mu$m and channel lengths $L_{SD}$ varying from 2 to 30 $\mu$m. The geometric scaling of the device resistance is shown in Fig. 2(b) which plots the log of the source to drain resistance versus log ($L_{SD}$) of the devices. The resistance data scale nonlinearly with channel length, and a least squares power law fit to the data yields $R \propto L^{1.76}$, This nonlinear scaling is most probably due to the nanotubes network and is an indication that the network approaches the percolation threshold where nonlinear effects are expected.26

The extracted contact resistance of our devices was thereby found to be as low as 11.18 k$\Omega$. Therefore, channel properties such as network density, which is crucial for long-channel devices, are not examined in the present work. It is worth noting at this level that all the measured transistor characteristics were found to achieve long-term stability operation under ambient conditions (i.e., within a maximum fluctuation of less than 4% after more than 2 months duration time). These performances are summarised in the Table I.

Finally, a sophisticated logic circuit based on the hybrid TFTs have also been demonstrated. An important outcome of this work is the addictiveness in integrating CMOS-like logic gates using ambipolar hybrid TFTs.

Figure 3 shows the output characteristics of the NOR gate. The logic block employs a 100 k$\Omega$ resistive load in the pull-down network, while four ambipolar hybrid TFTs were connected using external Au-wires to serve as the pull-up network. The value of the resistive load is chosen so that it is between the On-state resistance and the Off-state resistance of the transistors. The NOR circuit is operated with a $V_{DD}$ of 3 V. 3 and $-3$ V applying on gates A and B are treated as logics “1” and “0,” respectively. For the NOR gate, the output is “0” when either one of the two inputs is “1.” These output characteristics confirm that our circuits realize the logic function correctly. Based on such hybrid TFT transistors, the construction of truly integrated circuits is currently in progress.

In conclusion, we fabricated hybrid and air stable TFT ambipolar devices based on silicon carbide and carbon nanotubes materials, and we systematically studied their electronic properties. Combining the simultaneously p-type and n-type states into the hybrid devices, we demonstrated CMOS-NOR gates with appropriate resistive load. Although ambipolar behavior has been considered undesirable in next-generation devices, there is mounting evidence that the ability to control ambipolarity presents a design opportunities, and this work strongly argues for further investigation of its applicability.

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**FIG. 3.** Output characteristics of a NOR gate with resistive load using four hybrid ambipolar TFT. The supply voltage for the circuit is $V_{DD} = 3$ V. Input voltages of 3 and $-3$ V are treated as logics “1” and “0,” respectively.

**TABLE I.** Data summarizing the main transistor performances measured under ambient conditions with respect to the time over 2 months-duration.

<table>
<thead>
<tr>
<th></th>
<th>Day 1</th>
<th>Day 17</th>
<th>Day 33</th>
<th>Day 49</th>
<th>Day 65</th>
<th>% Fluctuation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_{on}$ (n-SiC) ($\mu$S)</td>
<td>19.6</td>
<td>19.8</td>
<td>20.2</td>
<td>20.1</td>
<td>20</td>
<td>£3%</td>
</tr>
<tr>
<td>$G_{on}$ (p-SWNT) ($\mu$S)</td>
<td>19.4</td>
<td>19.4</td>
<td>20.0</td>
<td>19.9</td>
<td>19.9</td>
<td>£3%</td>
</tr>
<tr>
<td>On/off switching ratios</td>
<td>$1.21 \times 10^5$</td>
<td>$1.17 \times 10^5$</td>
<td>$1.18 \times 10^5$</td>
<td>$1.3 \times 10^5$</td>
<td>$1.11 \times 10^5$</td>
<td>£1%</td>
</tr>
<tr>
<td>$S_{SWNT}$ (mV/decade)</td>
<td>121</td>
<td>126</td>
<td>122</td>
<td>123</td>
<td>125</td>
<td>£4%</td>
</tr>
<tr>
<td>$S_{SC}$ (mV/decade)</td>
<td>163</td>
<td>164</td>
<td>166</td>
<td>167</td>
<td>165</td>
<td>£3%</td>
</tr>
<tr>
<td>$R_{ON-FET}$ (k$\Omega$)</td>
<td>11.18</td>
<td>11.63</td>
<td>11.19</td>
<td>11.16</td>
<td>11.37</td>
<td>£4%</td>
</tr>
</tbody>
</table>
First, the electrical-percolation thresholds were systematically investigated with respect to the SWNT’s concentrations. Nanotube network having a surface density of 3.21 $\text{nm}^{-1}$ (i.e., the total length of SWNTs per unit area) and corresponding to eight drops cast onto the n-SiC substrate were then found to create a well percolated SWNT network with a high reproducibility.

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